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FORM FORM TRANSMITTAL FORM TO BE SECTION OF THE PROPERTY O			Application Number		09/344,169	
			Filing Date		June-24, 1999	
			First Named Inventor		William Eric Corr	
			Group Art Unit		2763	
MAY 2 4 2001			Examiner Name			
Total number of pages in this submission 2			Attorney Docket Number		await / P-3376	
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Leo Peters, Reg. No. 33,562, Phone: [+1] 408-433-4578						
Signature Lev Peters						
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I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope to: Assistant Commissioner for Patents, Washington, D,C. 20231 on this date:						
Typed or printed name Connie Del Castillo, Phone: [+1] 408-433-7191						
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Technology Center 2100

IN THE UNITED STACES PATENT AND TRADE ARK OFFICE

In re Application of:

William Eric Corr

Serial No.:

09/344,169

Group Art Un

2763

Filed:

June 24, 1999

For:

Determining Timing of Integrated

Circuits

Atty Docket:

await / P-3376

I hereby certify that this correspondence is being deposited with the U.S. Postal Service as First Class Mail in an envelope addressed to: Assitant Commissioner for Patents, Washington D.C. 20231, on the date indicated below:

Connie Del Castillo

5/21/01

nie dell



CERTIFICATION UNDER 37 C.F.R. 3.73(b)

Assistant Commissioner for Patents Washington, D.C. 20231

Sir:

LSI Logic Coporation, a Delaware corporation, certifies that it is the assignee of the entire right, title and interest in the patent application.

The undersigned has reviewed all the documents in the chain of title of the patent application identified above and, to the best of the undersigned's knowledge and belief, title is in the assignee identified above.

The undersigned (whose title is supplied below) is empowered to act on behalf of the assignee.

I hereby declare that all statements made herein of my own knowledge are true, and that all statements made on information and belief are believed to be true; and further, that these statements are made with the knowledge that willful false statements, and the like so made, are punishable by fine or imprisonment, or both, inder Section 1001, Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the application or any patent issuing thereon.

LSI Logic Corporation 1551 McCarthy Blvd., MS D-106 Milipitas, CA 95035 (408) 433-8708

Date: _ 5/18/01

Respectfully submitted,

Sandeep Jaggi Chief IP Counsel

Corporate Assistant Secretary LSI LOGIC CORPORATION